**February 10th Senior Project Meeting**

**Armstrong Hall 148: 2:00PM – 3:00PM**

**Members in Attendance:** All Members

* Zachary
  + Last Week
    - Created the presentation
    - Worked on the I2S/Filter Subsystem
    - Updated the top-level drawing
    - Created an updated schedule
    - Added all code to chip.v
      * All Verilog code is in chip.v and is synthesizable
      * Need help with a testbench
  + Next Week
    - Top-level testbench
    - Work on chip.v
* Whitley and Julie
  + Last Week
    - Register and I2C blocks working together
    - Loading register values works
  + Next Week
    - Top-level testbench
    - Implement FPGA for I2C
* Kevin
  + Last Week
    - Helped I2S/Filter module
    - EDA Tools tutorials
* Dhruvit
  + Last Week
  + Next Week
    - More verification of filter block